Eight Output Differential Buffer for PCIe Gen 2

ICS9DB803D

Description

The 9DB803 is a DB800 Version 2.0 Yellow Cover part with PCI Express Gen II support. It can be used in PC or embedded systems to provide outputs that have low cycle-to-cycle jitter (50ps), low output-to-output skew (100ps), and are PCI Express Gen 2 compliant. The 9DB803 supports a 1 to 8 output configuration, taking a spread or non spread differential HCSL input from a CK410(B) main clock such as 954101 and 932S401, or any other differential HCSL pair. 9DB803 can generate HCSL or LVDS outputs from 50 to 100MHz in PLL mode or 50 to 400Mhz in bypass mode. There are two de-jittering modes available selectable through the HIGH_BW# input pin, high bandwidth mode provides de-jittering for spread inputs and low bandwidth mode provides extra de-jittering for non-spread inputs. The SRC_IN#, PD#, and individual OE real-time input pins provide completely programmable power management control.

Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread.
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

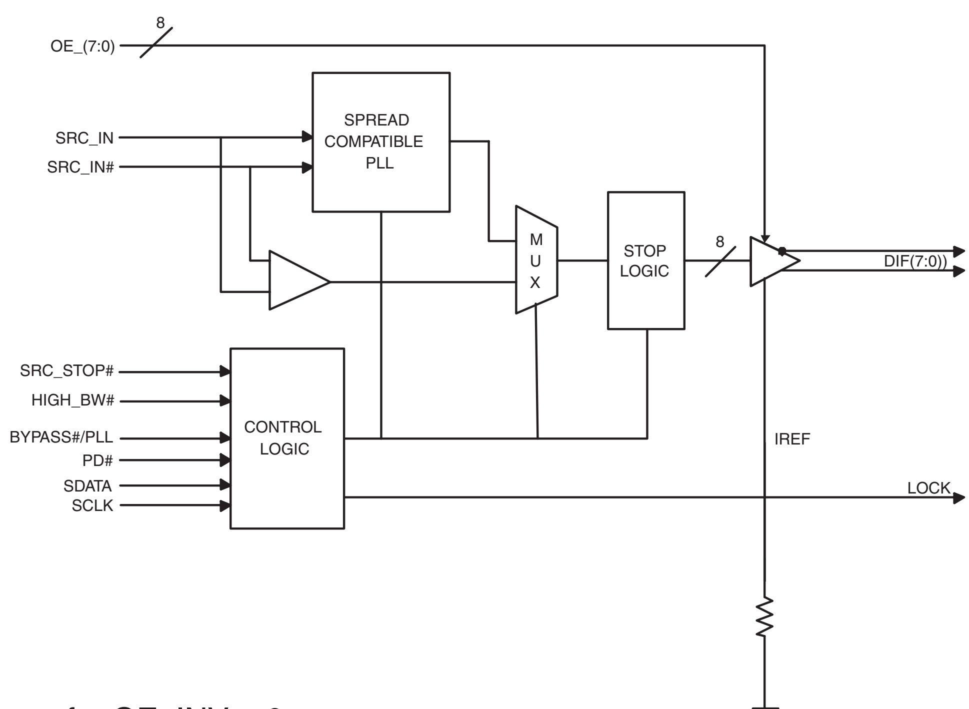
Output Features

- 8 - 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available

Key Specifications

- Outputs cycle-cycle jitter < 50ps
- Outputs skew: 50ps
- 50-100 MHz operation in PLL mode
- 50-400 MHz operation in Bypass mode
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.1ps rms
- 48-pin SSOP/TSSOP package
- Available in RoHS compliant packaging

Funtional Block Diagram



Note: Polarities shown for OE_INV = 0.

Pin Configuration

ICS9DB803 (Same as ICS9DB108)

SRC_DIV#	1	48	VDDA
VDD	2	47	GNDA
GND	3	46	IREF
SRC_IN	4	45	LOCK
SRC_IN#	5	44	OE_7
OE_0	6	43	OE_4
OE_3	7	42	DIF_7
DIF_0	8	41	DIF_7#
DIF_0#	9	40	**OE_INV**
GND	10	39	VDD
VDD	11	38	DIF_6
DIF_1	12	37	DIF_6#
DIF_1#	13	36	OE_6
OE_1	14	35	OE_5
OE_2	15	34	DIF_5
DIF_2	16	33	DIF_5#
DIF_2#	17	32	GND
GND	18	31	VDD
VDD	19	30	DIF_4
DIF_3	20	29	DIF_4#
DIF_3#	21	28	HIGH_BW#
BYPASS#/PLL	22	27	DIF_STOP#
SCLK	23	26	PD#
SDATA	24	25	GND

OE_INV = 0

ICS9DB803 (Same as ICS9DB801)

SRC_DIV#	1	48	VDDA
VDD	2	47	GNDA
GND	3	46	IREF
SRC_IN	4	45	LOCK
SRC_IN#	5	44	**OE7#**
OE0#	6	43	**OE4#**
OE3#	7	42	DIF_7
DIF_0	8	41	DIF_7#
DIF_0#	9	40	**OE_INV**
GND	10	39	VDD
VDD	11	38	DIF_6
DIF_1	12	37	DIF_6#
DIF_1#	13	36	**OE6#**
OE1#	14	35	**OE5#**
OE2#	15	34	DIF_5
DIF_2	16	33	DIF_5#
DIF_2#	17	32	GND
GND	18	31	VDD
VDD	19	30	DIF_4
DIF_3	20	29	DIF_4#
DIF_3#	21	28	HIGH_BW#
BYPASS#/PLL	22	27	**DIF_STOP**
SCLK	23	26	**PD**
SDATA	24	25	GND

OE_INV = 1

Polarity Inversion Pin List Table

Pins	OE_INV	
	0	1
6	OE_0	OE0#
7	OE_3	OE3#
14	OE_1	OE1#
15	OE_2	OE2#
26	PD#	PD
27	DIF_STOP#	DIF_STOP
35	OE_5	OE5#
36	OE_6	OE6#
43	OE_4	OE4#
44	OE_7	OE7#

Power Groups

Pin Number		Description
VDD	GND	
2	3	SRC_IN/SRC_IN#
6,11,19, 31,39	10,18, 25,32	DIF(7:0)
N/A	47	IREF
48	47	Analog VDD & GND for PLL core

Pin Description for OE_INV = 0

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SRC_DIV#	IN	Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC
2	VDD	PWR	Power supply, nominal 3.3V
3	GND	PWR	Ground pin.
4	SRC_IN	IN	0.7 V Differential SRC TRUE input
5	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
6	OE_0	IN	Active high input for enabling output 0. 0 = tri-state outputs, 1= enable outputs
7	OE_3	IN	Active high input for enabling output 3. 0 = tri-state outputs, 1= enable outputs
8	DIF_0	OUT	0.7V differential true clock output
9	DIF_0#	OUT	0.7V differential complement clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_1	OUT	0.7V differential true clock output
13	DIF_1#	OUT	0.7V differential complement clock output
14	OE_1	IN	Active high input for enabling output 1. 0 = tri-state outputs, 1= enable outputs
15	OE_2	IN	Active high input for enabling output 2. 0 = tri-state outputs, 1= enable outputs
16	DIF_2	OUT	0.7V differential true clock output
17	DIF_2#	OUT	0.7V differential complement clock output
18	GND	PWR	Ground pin.
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_3	OUT	0.7V differential true clock output
21	DIF_3#	OUT	0.7V differential complement clock output
22	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
23	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
24	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.

Pin Description for OE_INV = 0

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	GND	PWR	Ground pin.
26	PD#	IN	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped.
27	DIF_STOP#	IN	Active low input to stop differential output clocks.
28	HIGH_BW#	PWR	3.3V input for selecting PLL Band Width 0 = High, 1= Low
29	DIF_4#	OUT	0.7V differential complement clock output
30	DIF_4	OUT	0.7V differential true clock output
31	VDD	PWR	Power supply, nominal 3.3V
32	GND	PWR	Ground pin.
33	DIF_5#	OUT	0.7V differential complement clock output
34	DIF_5	OUT	0.7V differential true clock output
35	OE_5	IN	Active high input for enabling output 5. 0 = tri-state outputs, 1= enable outputs
36	OE_6	IN	Active high input for enabling output 6. 0 = tri-state outputs, 1= enable outputs
37	DIF_6#	OUT	0.7V differential complement clock output
38	DIF_6	OUT	0.7V differential true clock output
39	VDD	PWR	Power supply, nominal 3.3V
40	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
41	DIF_7#	OUT	0.7V differential complement clock output
42	DIF_7	OUT	0.7V differential true clock output
43	OE_4	IN	Active high input for enabling output 4. 0 = tri-state outputs, 1= enable outputs
44	OE_7	IN	Active high input for enabling output 7. 0 = tri-state outputs, 1= enable outputs
45	LOCK	OUT	3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.
46	IREF	IN	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

Pin Description for OE_INV = 1

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	SRC_DIV#	IN	Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC
2	VDD	PWR	Power supply, nominal 3.3V
3	GND	PWR	Ground pin.
4	SRC_IN	IN	0.7 V Differential SRC TRUE input
5	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
6	OE0#	IN	Active low input for enabling DIF pair 0. 1 = tri-state outputs, 0 = enable outputs
7	OE3#	IN	Active low input for enabling DIF pair 3. 1 = tri-state outputs, 0 = enable outputs
8	DIF_0	OUT	0.7V differential true clock output
9	DIF_0#	OUT	0.7V differential complement clock output
10	GND	PWR	Ground pin.
11	VDD	PWR	Power supply, nominal 3.3V
12	DIF_1	OUT	0.7V differential true clock output
13	DIF_1#	OUT	0.7V differential complement clock output
14	OE1#	IN	Active low input for enabling DIF pair 1. 1 = tri-state outputs, 0 = enable outputs
15	OE2#	IN	Active low input for enabling DIF pair 2. 1 = tri-state outputs, 0 = enable outputs
16	DIF_2	OUT	0.7V differential true clock output
17	DIF_2#	OUT	0.7V differential complement clock output
18	GND	PWR	Ground pin.
19	VDD	PWR	Power supply, nominal 3.3V
20	DIF_3	OUT	0.7V differential true clock output
21	DIF_3#	OUT	0.7V differential complement clock output
22	BYPASS#/PLL	IN	Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode
23	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
24	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.

Pin Description for OE_INV = 1

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
25	GND	PWR	Ground pin.
26	PD	IN	Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped.
27	DIF_STOP	IN	Active High input to stop differential output clocks.
28	HIGH_BW#	PWR	3.3V input for selecting PLL Band Width 0 = High, 1= Low
29	DIF_4#	OUT	0.7V differential complement clock output
30	DIF_4	OUT	0.7V differential true clock output
31	VDD	PWR	Power supply, nominal 3.3V
32	GND	PWR	Ground pin.
33	DIF_5#	OUT	0.7V differential complement clock output
34	DIF_5	OUT	0.7V differential true clock output
35	OE5#	IN	Active low input for enabling DIF pair 5. 1 = tri-state outputs, 0 = enable outputs
36	OE6#	IN	Active low input for enabling DIF pair 6. 1 = tri-state outputs, 0 = enable outputs
37	DIF_6#	OUT	0.7V differential complement clock output
38	DIF_6	OUT	0.7V differential true clock output
39	VDD	PWR	Power supply, nominal 3.3V
40	OE_INV	IN	This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#)
41	DIF_7#	OUT	0.7V differential complement clock output
42	DIF_7	OUT	0.7V differential true clock output
43	OE4#	IN	Active low input for enabling DIF pair 4 1 = tri-state outputs, 0 = enable outputs
44	OE7#	IN	Active low input for enabling DIF pair 7. 1 = tri-state outputs, 0 = enable outputs
45	LOCK	OUT	3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved.
46	IREF	IN	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
47	GNDA	PWR	Ground pin for the PLL core.
48	VDDA	PWR	3.3V power for the PLL core.

Absolute Max

Symbol	Parameter	Min	Max	Units
VDD_A	3.3V Core Supply Voltage		4.6	V
VDD_In	3.3V Logic Supply Voltage		4.6	V
V_{IL}	Input Low Voltage	GND-0.5		V
V_{IH}	Input High Voltage		V_{DD}+0.5V	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	3.3 V +/-5%	GND - 0.3		0.8	V	
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	
Operating Supply Current	$I_{DD3.3OP}$	Full Active, C_L = Full load;			200	mA	
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven			60	mA	
		all differential pairs tri-stated			6	mA	
Input Frequency	F_{iPLL}	PLL Mode	50		110	MHz	1
	$F_{iBYPASS}$	Bypass Mode	50		400	MHz	1
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs	1.5		5	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
PLL Bandwidth	BW	PLL Bandwidth when PLL_BW=0	2	3	4	MHz	1
		PLL Bandwidth when PLL_BW=1	0.7	1	1.4	MHz	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Modulation Frequency	f_{MOD}	Triangular Modulation	30		33	kHz	1
Tdrive_SRC_STOP#	t_{DRVSTP}	DIF output enable after SRC_Stop# de-assertion			10	ns	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of PD# and SRC_STOP#			5	ns	1
Trise	t_R	Rise time of PD# and SRC_STOP#			5	ns	2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Time from deassertion until outputs are >200 mV

Electrical Characteristics - Clock Input Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input High Voltage - DIF_IN	V_{IHDIF}	Differential inputs (single-ended measurement)	600	800	1150	mV	1
Input Low Voltage - DIF_IN	V_{ILDIF}	Differential inputs (single-ended measurement)	V_{SS} - 300	0	300	mV	1
Input Common Mode Voltage - DIF_IN	V_{COM}	Common Mode Input Voltage	300		1000	mV	1
Input Amplitude - DIF_IN	V_{SWING}	Peak to Peak value	300		1450	mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	1
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through Vswing min centered around differential zero

Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, R_{REF}=475Ω

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo[1]	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1
Min Voltage	Vuds		-300				1
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175		700	ps	1
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175		700	ps	1
Rise Time Variation	d-t_r				125	ps	1
Fall Time Variation	d-t_f				125	ps	1
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50	55	%	1
Skew	t_{sk3}	V_T = 50%			50	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		40	50	ps	1,5
		BYPASS mode as additive jitter		15	50	ps	1,5
Jitter, Phase	$t_{jphasebypass}$	PCIe Gen 1 specs (pk to pk value)		30	86	ps	1,6,7
		PCIe Gen 2 specs (rms value)		2.6	3.1	ps	1,6,7
	$t_{jphasePLL}$	PCIe Gen 1 specs (pk to pk value)		40	86	ps	1,6,7
		PCIe Gen 2 specs (rms value)		2.8	3.1	ps	1,6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Applies to Bypass Mode Only

[5] Measured from differential waveform

[6] See http://www.pcisig.com for complete specs

[7] Device driven by HP81134A Pulse Generator

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	DIF 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2,3
	DIF 133	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns	1,2,4
	DIF 166	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns	1,2,4
	DIF 200	4.91450	4.99950	4.99950	5.00000	5.00050	5.02563	5.11063	ns	1,2,4
	DIF 266	3.66463	3.74963	3.74963	3.75000	3.75038	3.76922	3.85422	ns	1,2,4
	DIF 333	2.91470	2.99970	2.99970	3.00000	3.00030	3.01538	3.10038	ns	1,2,4
	DIF 400	2.41475	2.49975	2.49975	2.50000	2.50025	2.51282	2.59782	ns	1,2,4

Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Period		
		Minimum Absolute Period	Minimum Absolute Period	Minimum Absolute Period	Nominal	Maximum	Maximum	Maximum	Units	Notes
Signal Name	DIF 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2,3
	DIF 133	7.41425		7.49925	7.50000	7.50075		7.62345	ns	1,2,4
	DIF 166	5.91440		5.99940	6.00000	6.00060		6.11576	ns	1,2,4
	DIF 200	4.91450		4.99950	5.00000	5.00050		5.11063	ns	1,2,4
	DIF 266	3.66463		3.74963	3.75000	3.75038		3.85422	ns	1,2,4
	DIF 333	2.91470		2.99970	3.00000	3.00030		3.10038	ns	1,2,4
	DIF 400	2.41475		2.49975	2.50000	2.50025		2.59782	ns	1,2,4

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PLL or Bypass mode

[4] Driven by CPU output of CK410/CK505 main clock, **Bypass mode only**

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, Route as non-coupled 50 ohm trace.	0.5 max	inch	1
L2 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1
L3 length, Route as non-coupled 50 ohm trace.	0.2 max	inch	1
Rs	33	ohm	1
Rt	49.9	ohm	1

Down Device Differential Routing	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	2 min to 16 max	inch	1
L4 length, Route as coupled **stripline** 100 ohm differential trace.	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector	Dimension or Value	Unit	Figure
L4 length, Route as coupled **microstrip** 100 ohm differential trace.	0.25 to 14 max	inch	2
L4 length, Route as coupled **stripline** 100 ohm differential trace.	0.225 min to 12.6 max	inch	2

Figure 1 Down device routing.

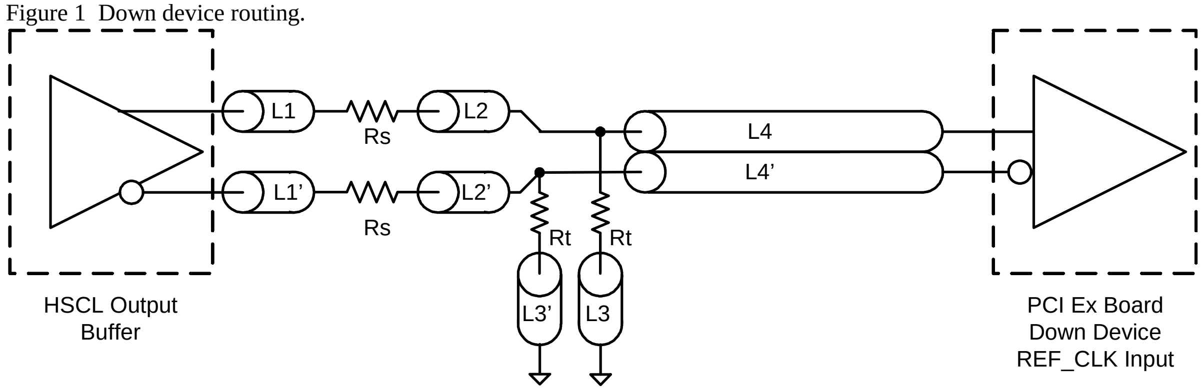


Figure 1

Figure 2 PCI Express Connector Routing.

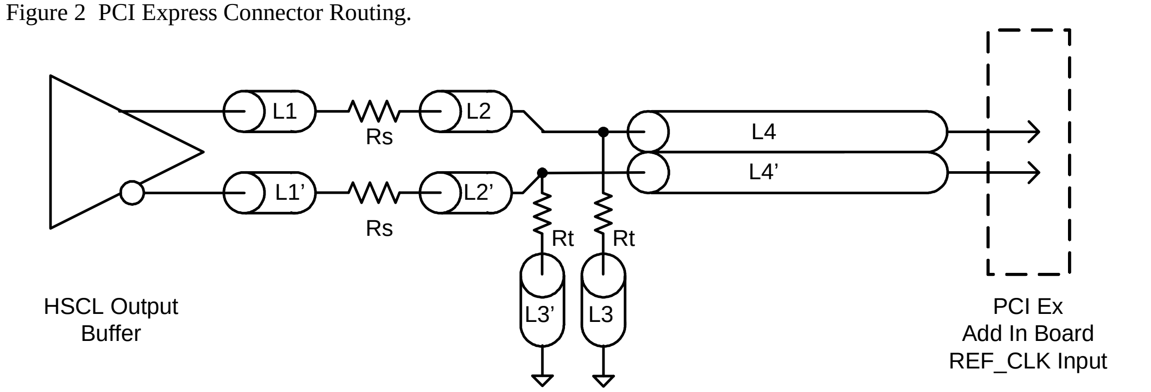


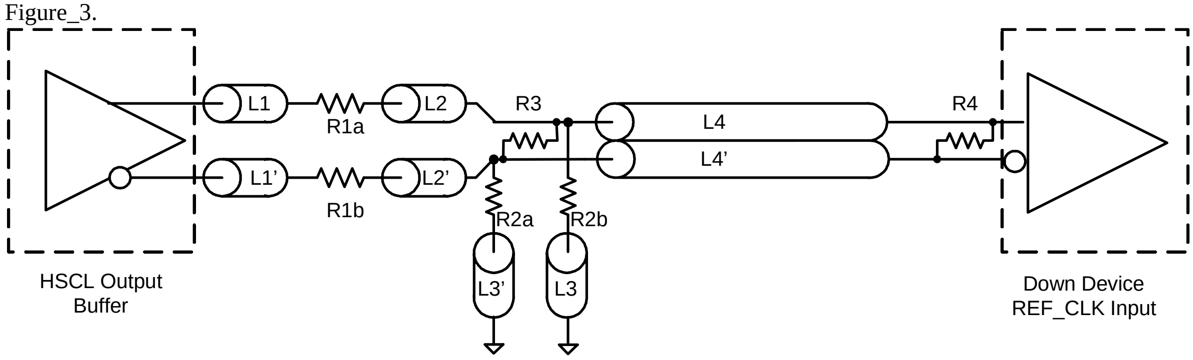
Figure 2

Alternative termination for LVDS and other common differential signals. Figure 3.

Vdiff	Vp-p	Vcm	R1	R2	R3	R4	Note
0.45 v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1

Figure_3.



R2a = R2b = R2

Cable connected AC coupled application, figure 4

Component	Value	Note
R5a,R5b	8.2K 5%	
R6a,R6b	1K 5%	
Cc	0.1 uF	
Vcm	0.350 volts	

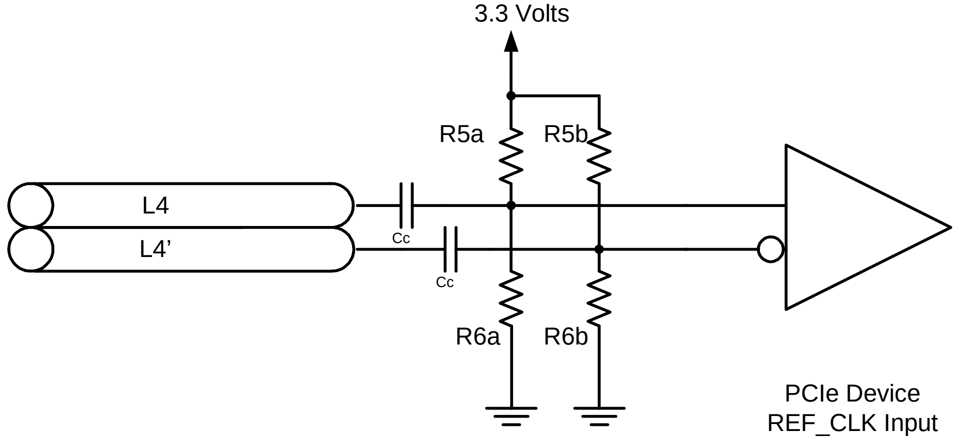


Figure_4.

General SMBus serial interface information for the ICS9DB803D

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC $_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC $_{(h)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD $_{(h)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(h)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address DC$_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address DC$_{(h)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address DD$_{(h)}$			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PD_Mode	PD# drive mode	RW	driven	Hi-Z	0
Bit 6	-	STOP_Mode	SRC_Stop# drive mode	RW	driven	Hi-Z	0
Bit 5	-	PD_Polarity	Select PD polarity	RW	Low	High	0
Bit 4	-	Reserved	Reserved	RW	Reserved		X
Bit 3	-	Reserved	Reserved	RW	Reserved		X
Bit 2	-	PLL_BW#	Select PLL BW	RW	High BW	Low BW	1
Bit 1	-	BYPASS#	BYPASS#/PLL	RW	fan-out	ZDB	1
Bit 0	-	SRC_DIV#	SRC Divide by 2 Select	RW	x/2	1x	1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	42,41	DIF_7	Output Control	RW	Disable	Enable	1
Bit 6	38,37	DIF_6	Output Control	RW	Disable	Enable	1
Bit 5	34,33	DIF_5	Output Control	RW	Disable	Enable	1
Bit 4	30,29	DIF_4	Output Control	RW	Disable	Enable	1
Bit 3	20,21	DIF_3	Output Control	RW	Disable	Enable	1
Bit 2	16,17	DIF_2	Output Control	RW	Disable	Enable	1
Bit 1	12,13	DIF_1	Output Control	RW	Disable	Enable	1
Bit 0	8,9	DIF_0	Output Control	RW	Disable	Enable	1

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	42,41	DIF_7	Output Control	RW	Free-run	Stoppable	0
Bit 6	38,37	DIF_6	Output Control	RW	Free-run	Stoppable	0
Bit 5	34,33	DIF_5	Output Control	RW	Free-run	Stoppable	0
Bit 4	30,29	DIF_4	Output Control	RW	Free-run	Stoppable	0
Bit 3	20,21	DIF_3	Output Control	RW	Free-run	Stoppable	0
Bit 2	16,17	DIF_2	Output Control	RW	Free-run	Stoppable	0
Bit 1	12,13	DIF_1	Output Control	RW	Free-run	Stoppable	0
Bit 0	8,9	DIF_0	Output Control	RW	Free-run	Stoppable	0

SMBus Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7		Reserved		RW	Reserved		X
Bit 6		Reserved		RW	Reserved		X
Bit 5		Reserved		RW	Reserved		X
Bit 4		Reserved		RW	Reserved		X
Bit 3		Reserved		RW	Reserved		X
Bit 2		Reserved		RW	Reserved		X
Bit 1		Reserved		RW	Reserved		X
Bit 0		Reserved		RW	Reserved		X

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBus Table: DEVICE ID

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)		RW	Device ID is 83 Hex for 9DB803 and 43 Hex for 9DB403		0
Bit 6	-	Device ID 6		RW			X
Bit 5	-	Device ID 5		RW			X
Bit 4	-	Device ID 4		RW			0
Bit 3	-	Device ID 3		RW			0
Bit 2	-	Device ID 2		RW			0
Bit 1	-	Device ID 1		RW			1
Bit 0	-	Device ID 0		RW			1

SMBus Table: Byte Count Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

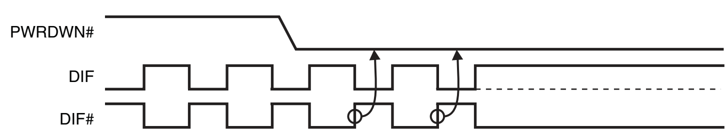
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

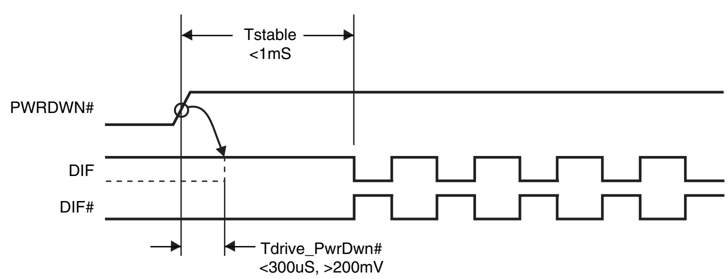
PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to ‘0’, all clock outputs will be held with DIF driven High with 2 x I_{REF} and DIF# tri-stated. If the PD# drive mode bit is set to ‘1’, both DIF and DIF# are tri-stated.



PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to ‘1’, all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.



SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

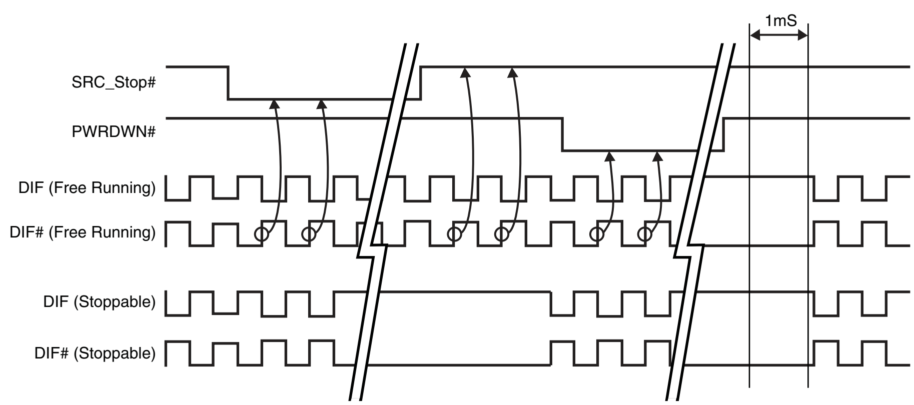
SRC_STOP# - Assertion

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6xI_{REF}. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

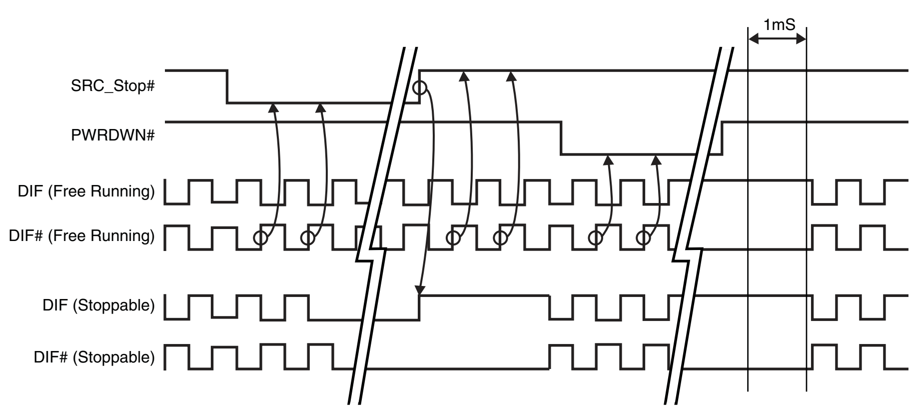
SRC_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

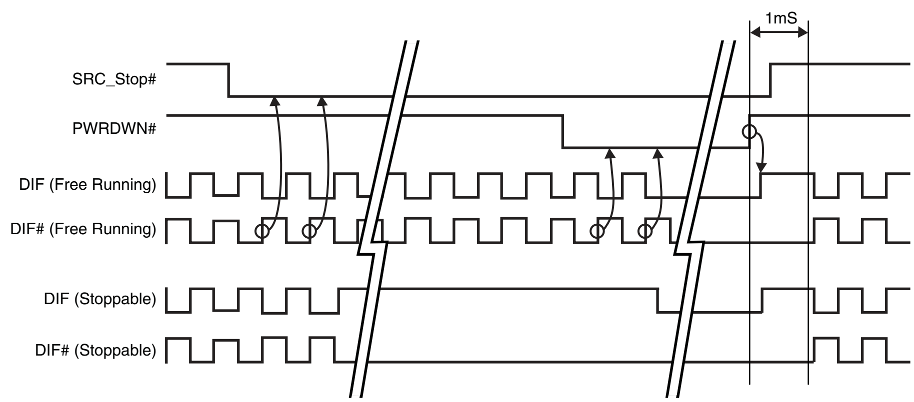
SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)



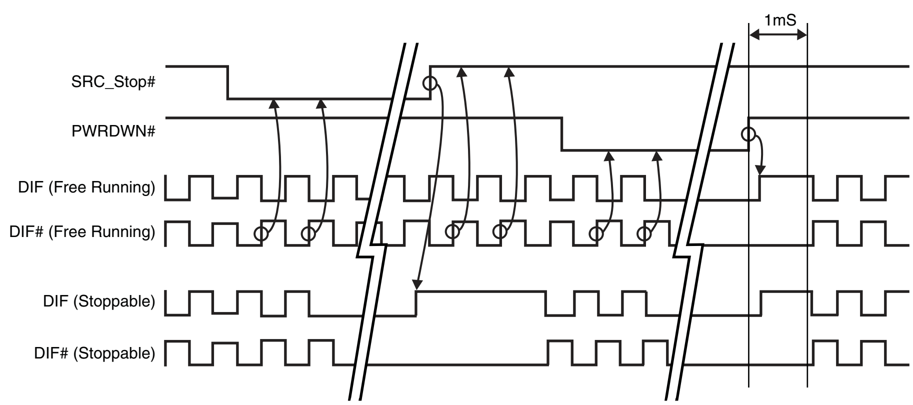
SRC_STOP_2 (SRC_Stop =Tristate, PD = Driven)

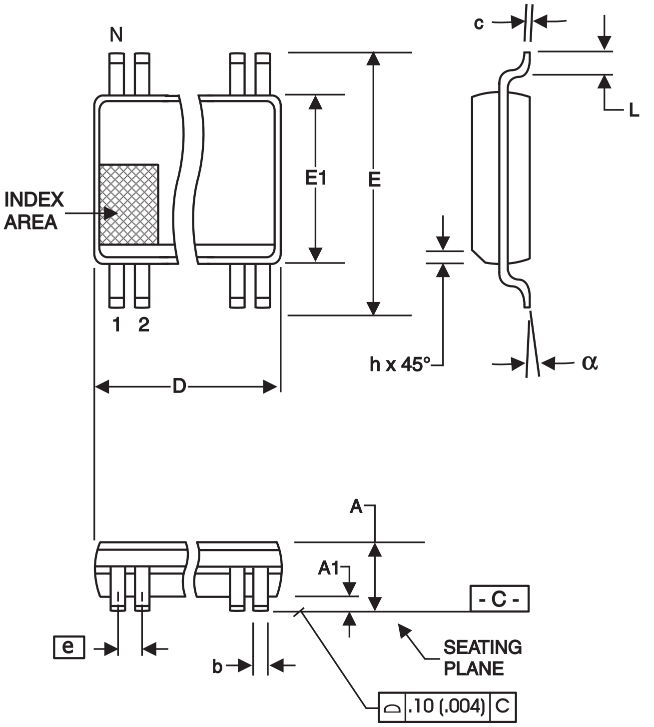


SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)



SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)





SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

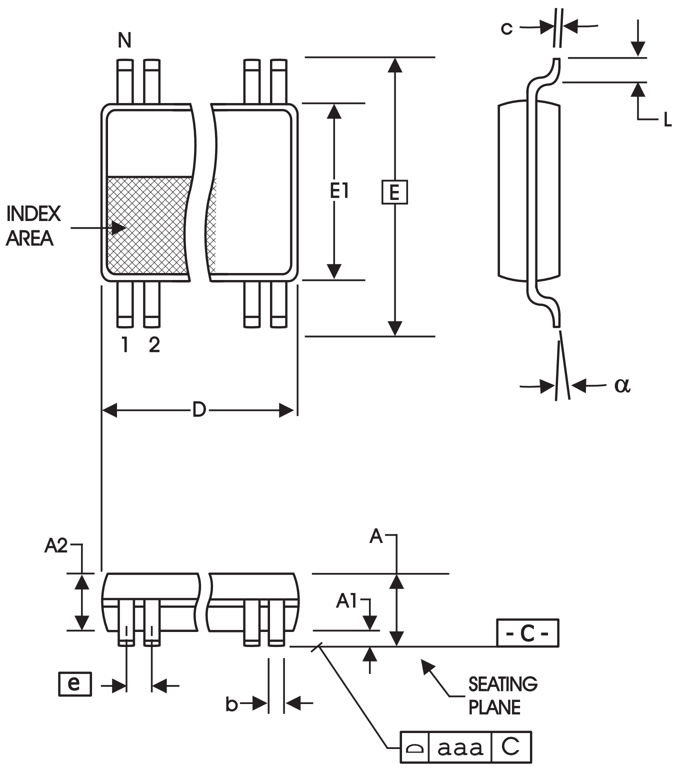
Ordering Information

ICS9DB803DFLFT

Example:

ICS XXXX D F LF T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Lead Free, RoHS Compliant (Optional)**
- **F** — **Package Type**
  F = SSOP
- **D** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type (consists of 3 to 7 digit numbers)**
- **ICS** — **Prefix**
  ICS = Standard Device



48-Lead, 6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS9DB803DGLFT

Example:

ICS XXXX D G LF T

- **T** — **Designation for tape and reel packaging**
- **LF** — **Lead Free, RoHS Compliant (Optional)**
- **G** — **Package Type**
  G = TSSOP
- **D** — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type (consists of 3 to 7 digit numbers)**
- **ICS** — **Prefix**
  ICS = Standard Device

Revision History

Rev.	Issue Date	Description	Page #
B	8/23/2007	Fixed Frequency typo Description.	1
C	2/29/2008	Added Input Clock Specs	8
D	3/18/2008	Fixed typo in Input Clock Parameters	8
F	4/10/2008	Updated Input Clock Specs	8

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